CLAIMS

- 1. (Canceled)
- 2. (Currently amended) The method of claim 1 wherein the step of detecting further emprises: In a wireless receiver wherein a radio frequency signal is received, downconverted, and processed into in-phase (I) and quadrature (Q) signal paths, a method of automatic gain control (AGC) comprising:
- (a) at a specified stage in an I/Q baseband strip containing multiple automatic gain control (AGC) stages, each of said AGC stages having locally generated control signals associated therewith:
 - i. detecting respective I and Q output signals received from respective I and Q variable gain amplifiers (VGAs) associated with said specified AGC stage;
 - (a) <u>ii.</u> passing said respective I and Q output signals through respective high pass filters (HPFs);
 - (b) <u>iii.</u> rectifying said respective I and Q filtered output signals;
 - (e) iv. adding said respective I and Q filtered output signals in an operational amplifier; and
 - (d) \underline{v} . passing said added I and Q filtered output signal through a low pass filter (LPF);
 - vi. digitizing said detected I and Q signals; and
 - vii. adjusting with said associated control signal said respective I and Q VGAs for differences between said detected I and Q output signals and a reference signal; and (b) repeating (a) through each AGC stage.
- 3. (Currently amended) The method of claim ± 2 wherein the step of digitizing further comprises:
- (a) receiving in an analogue to digital converter (ADC) said added low pass filtered I and Q signal;
 - (b) comparing said received signals to a reference signal; and
 - (c) generating digital up/down and count/hold control signals.

- 4. (Original) The method of claim 3 wherein said step of comparing further comprises using a multi-level comparator and a logic circuit to generate said digital up/down and count/hold control signals.
 - 5. (Original) The method of claim 4 wherein the step of adjusting further comprises:
 - (a) receiving in an up/down counter said up/down and count/hold control signals; and
 - (b) setting the gains of respective I and Q variable gain amplifiers (VGAs).
 - 6. (Original) The method of claim 5 wherein the step of setting further comprises:
- (a) if said I and Q filtered output signals fall outside a predefined boundary, modifying the gains of said respective I and Q VGAs until a desired I/Q output signal is achieved;
 - (b) else, maintaining said respective I and Q VGA settings.
- 7. (Original) The method of claim 6 wherein the step of modifying comprises adjusting said respective I and Q VGAs at a fast rate if said detected I/Q output signal is beyond a first predefined range or at a slow rate if said detected I/Q output signal is beyond a second predefined range.
- 8. (Original) The method of claim 6 wherein the step of modifying comprises adjusting said respective I and Q VGAs at a large magnitude if said detected I/Q output signal is beyond a first predefined range or at a small magnitude if said detected I/Q output signal is beyond a second predefined range.

9. (Canceled)

- 10. (Currently amended) The automatic gain control circuit of claim 9 In a wireless receiver where a radio frequency signal is received, downconverted, and processed into in-phase (I) and quadrature (Q) signal paths, an automatic gain control (AGC) circuit comprising multiple AGC stages where each of the AGC stages includes:
 - (a) respective I and Q variable gain amplifiers (VGAs);

- (b) a detector to detect respective I and Q output signals received from the respective I and Q VGAs;
- (c) an analog to digital converter (ADC) to convert the detected I and Q output signals; and
- (d) a digital engine to digitally adjust the respective I and Q VGAs for differences between the detected I and Q output signals and a reference signal;

wherein said the detector comprises:

- i. respective I and Q high pass filters (HPFs) for removing to remove direct current (DC) offsets from said the respective I and Q output signals;
- ii. a rectifier communicating with said the respective I and Q HPFs for changing said to change the respective filtered I and Q output signals from alternating current (AC) to direct current (DC);
- iii. an operational amplifier (Op-amp) communicating with said the rectifier for adding said to add the filtered I and Q output signals; and
- iv. a low pass filter (LPF) communicating with said the Op-amp for filtering said to filter the added I and Q output signals.
- 11. (Original) The automatic gain control circuit of claim 10 wherein said ADC comprises a multi-level comparator and a logic circuit.
- 12. (Original) The automatic gain control circuit of claim 11 wherein the number of levels in said multi-level comparator is at least four.
- 13. (Original) The automatic gain control circuit of claim 12 wherein said digital engine comprises an up/down counter for setting gains associated with said respective I and Q variable gain amplifiers (VGAs).

14.-19. (Canceled)

20. (New) A wireless receiver including a plurality of serially connected automatic gain control stages, each stage comprising:

PAGE 4 OF 9 DO. NO. 9931-042 SERIAL NO. 10/661,945 I and Q variable gain amplifiers to generate I and Q signals, respectively; a detector to generate a detect signal by detecting a difference between the I and Q signals;

an ADC to convert the detect signal to a digital detect signal; and an engine to generate a control signal responsive to the digital detect signal and a reference signal;

where the I and Q VGAs operate responsive to the control signal.

- 21. (New) The wireless receiver of claim 20 comprising: I and Q buffers to buffer the I and Q signals, respectively.
- 22. (New) The wireless receiver of claim 20 where the detector includes:

 I and Q high pass filters to generate I and Q filtered signals by removing direct current offsets from the I and Q output signals.
- 23. (New) The wireless receiver of claim 22 where the detector includes: a rectifier communicating with the I and Q high pass filters to change the I and Q filtered signals from alternating current to direct current.
- 24. (New) The wireless receiver of claim 23 where the detector includes: an operational amplifier to generate added I and Q signals by adding the I and Q filtered signals.
 - 25. (New) The wireless receiver of claim 24 where the detector includes: a low pass filter to filter the added I and Q signals.
 - 25. (New) A method comprising;

generating a detect signal by detecting a difference between I and Q signals at respective outputs of I and Q variable gain amplifiers of a plurality of serially connected automatic gain control stages;

converting the detect signal to a digital detect signal;

Do. No. 9931-042 Serial No. 10/661,945 generating a control signal to control the I and Q variable gain amplifiers responsive to the digital detect signal; and

adjusting the I and Q variable gain amplifiers responsive to the control signal.

- 26. (New) The method of claim 25 comprising: generating I and Q filtered signals by removing direct current offsets from the I and Q output signals.
 - 27. (New) The method of claim 26 comprising: rectifying the I and Q filtered signals from alternating current to direct current.
 - 28. (New) The method of claim 27 comprising: adding the rectified I and Q signals.
 - 29. (New) The method of claim 28 comprising: low pass filtering the added I and Q signals.